

**REMARKS**

The Examiner has restricted the invention of the subject application to one of the following inventions:

- I. Claims 1-6, drawn to a process for forming a CMOS device, classified in class 458, subclass 592;
- II. Claims 7-11, drawn to a process for forming a gate metal silicide for CMOS devices, classified in class 438, subclass 592;
- III. Claims 12-17, drawn to a process for forming a gate metal silicide for CMOS devices prior to gate definition, classified in class 438, subclass 592;
- IV. Claims 18-19, drawn to a process for forming a replacement gate structure for CMOS devices, classified in class 438, subclass 592; and
- V. Claim 20, drawn to a process for forming an interconnect on a dual metal replacement gate structure for connection of nFET and pFET gates of a CMOS device, classified in class 438, subclass 592.

Applicants respectfully disagree that these groups represent different inventions requiring different searches.

The claims of Group I are drawn to a method of forming a CMOS device including a gate metal silicide. The claims of Group II are drawn to forming a gate metal silicide for CMOS devices. The claims of Group III are drawn to forming a gate metal silicide for CMOS devices prior to gate definition. The claims of Group IV are drawn to a method of forming a replacement gate structure, which includes a gate metal silicide. The claims of Group V are drawn to a method of forming an

interconnect for the connection of gates on a CMOS device, including a gate metal silicide.

It is respectfully submitted that the groups are therefore co-extensive and Applicants respectfully submit that a search pertaining to one of the above-identified groups would necessarily encompass subject matter of the other group and separate searches for each group would be unwarranted and duplicative. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the requirement for restriction.

Reconsideration and withdrawal of the restriction requirement and an action on the merits of all the claims are respectfully requested.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date indicated below as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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